AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A semiconductor device comprising:

a semiconductor substrate having a pattern forming region and a pattern non-forming region;

a wiring pattern formed on said pattern forming region;

a plurality of dummy patterns formed on said pattern non-forming region, said plurality of dummy patterns being formed within a plurality of dummy areas, and each of the plurality of dummy areas having a same shape; and

an insulating film formed on said wiring pattern and said plurality of dummy patterns;

wherein said insulating film is formed by a chemical vapor deposition and is smoothed by chemical mechanical polishing; ~~and~~

wherein each of said plurality of dummy patterns has a plurality of line patterns, and each of said plurality of line patterns is spaced apart from each other by an area filled by the deposition of said insulating film; and~~.~~

wherein a distance between each of said plurality of line patterns is less than 72 μm.

2-4. (Cancelled)

5. (Previously Presented) A semiconductor device according to claim 1, wherein the dummy areas each have a square shape.

6. (Previously Presented) A semiconductor device according to claim 1, wherein the dummy areas are arranged in lattice form.

7. (Cancelled)

8. (Previously Presented) A semiconductor device according to claim 1, wherein said plurality of dummy patterns are line patterns.

9. (Currently Amended) A semiconductor device comprising:

a semiconductor substrate having a pattern area and a non-pattern area;

a conductive pattern formed on said pattern area of said semiconductor substrate; and

a plurality of dummy patterns formed on said non-pattern area of said semiconductor substrate, each of said plurality of dummy patterns having a same continuous rectangular outline shape as each other and being arranged in a matrix with predetermined spacing; and

an insulating film formed on said ~~writing~~ conductive pattern and said plurality of dummy patterns;

wherein said insulating film is formed by a chemical vapor deposition and is smoothed by chemical mechanical polishing; ~~and~~

wherein each of said plurality of dummy patterns has an opening so that a pattern ratio of said semiconductor device is reduced.; and

wherein a width of the opening of each of said plurality of dummy patterns is less than 72 μm.

10. (Previously Presented) A semiconductor device according to claim 9, wherein each of said plurality of dummy patterns has a square outline.

11. (Previously Presented) A semiconductor device according to claim 9, wherein the opening has a square outline.

12. (Previously Presented) A semiconductor device according to claim 9, wherein the opening has a shape of a letter.

13. (Previously Presented) A semiconductor device according to claim 9, wherein the opening has a shape of a plurality of letters.

14. (Currently amended) A semiconductor device comprising:

a semiconductor substrate having a pattern area and a non-pattern area;

a conductor pattern formed on said pattern area of said semiconductor substrate;

a plurality of dummy patterns formed on said non-pattern area of said semiconductor substrate;

an insulating film formed on said conductive pattern and said plurality of dummy patterns;

wherein said insulating film is formed by a chemical vapor deposition and is smoothed by chemical mechanical polishing;

wherein each of said plurality of dummy patterns are formed in a plurality of dummy areas, each of ~~the~~ said plurality of dummy areas having a same shape, and each of said plurality of dummy patterns being arranged in a matrix with predetermined spacing;

wherein each of said plurality of dummy patterns has a space portion within each of the dummy areas so that a pattern ratio of said semiconductor device is reduced; and

wherein each space portion of said plurality of dummy patterns indicates a shape of at least one of a letter and graphic, and each space portion of said plurality of dummy patterns has a width less than 72 μm.

15. (Previously Presented) A semiconductor device according to claim 14, wherein each of said plurality of dummy patterns has a rectangular outline and an opening at the space portion.

16. (Previously Presented) A semiconductor device according to claim 15, wherein the opening has a square outline.

17. (Previously Presented) A semiconductor device according to claim 15, wherein the opening has a shape of a letter.

18. (Previously Presented) A semiconductor device according to claim 15, wherein the opening has a shape of a plurality of letters.

19. (Previously Presented) A semiconductor device according to claim 14, wherein said plurality of dummy patterns are line patterns, and each of the dummy areas has line patterns spaced apart from each other.

20. (Previously Presented) A semiconductor device according to claim 19, wherein the line patterns are arranged with a space therebetween being approximately less than 72 μm.

21. (Previously Presented) A semiconductor device according to claim 1, wherein said line patterns are arranged in a same direction.